

REV	DESCRIPTION	DATE	APPROVED
A	Initial schematic ready for layout - Alpha Release	04/01/07	RRP
B	Pre-production release - Beta Release	07/01/07	RRP
C	Production release for 0.50 mm	09/01/07	RRP
D	Pre-production release for 0.65 mm	09/28/07	RRP

Memory Address Table		
CHIP SELECT	BASE ADDRESS HEX	FUNCTION
CE0 - NAND CS0	0x0200 0000	NAND FLASH CS0 R/W
CE0 - NAND CS1	0x0200 4000	NAND FLASH CS1 R/W
CE1 - PHY/MAC CHIP	0x0401 4000	DM9000A READ WRITE

ARM ADDRESSING															
A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	WORD
	X	X	1	1	1	1	1	1	1	1	1	1	1	1	1
					F				F				F		

I2C Address Table			
ADDRESS HEX	BINARY	DEVICE	FUNCTION
0x25	00100011B	MSP430	RTC,IR CTL, IO CTL, POWER MONITOR
0x1B	00011011B	AIC33	AUDIO CODEC - 00110(MFP1)(MFP0)
0x5D	01011101B	TVP5146	VIDEO DECODER - 101110(I2CA)

SCHEMATIC CONTENTS

- SHEET01 - TITLE
- SHEET02 - DM355 SERIAL I/O
- SHEET03 - DM355 DDR2 INTERFACE
- SHEET04 - DM355 EMIF
- SHEET05 - DM355 USB
- SHEET06 - DM355 VIDEO
- SHEET07 - DM355 JTAG,CLKS,RESET
- SHEET08 - DM355 POWER/GND-pins
- SHEET09 - DM355 DECOUPLING CAPS

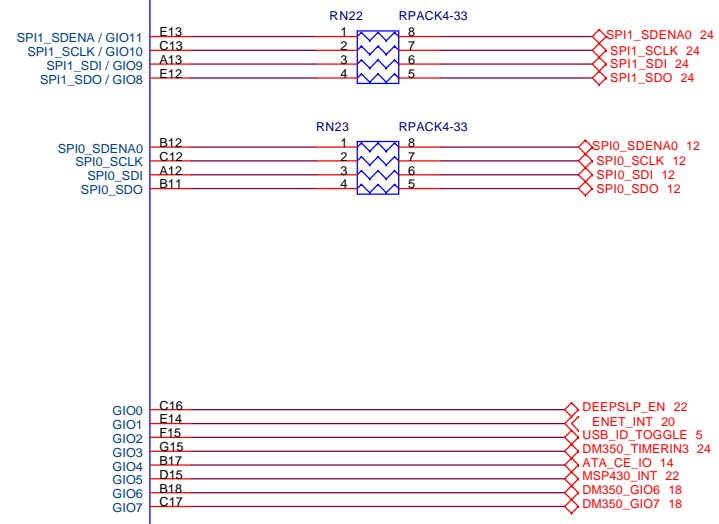
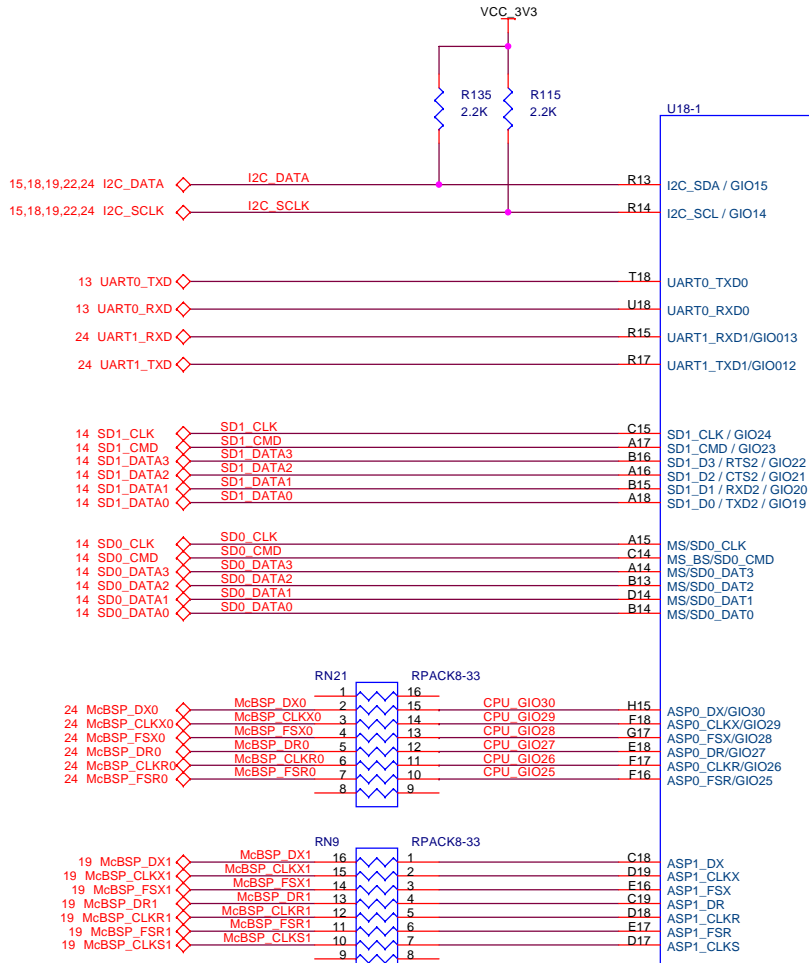
- SHEET10 - DDR2 MEMORY
- SHEET11 - JTAG CONNECTORS
- SHEET12 - NAND FLASH, SPI EEPROM, EMIF I/O DC
- SHEET13 - RS232 INTERFACE
- SHEET14 - SD/MMC IF - CE ATA IF
- SHEET15 - VIDEO INPUT MULTIPLEXER
- SHEET16 - IMAGER INTERFACE
- SHEET17 - 5146 DECODER
- SHEET18 - VIDEO DAUGHTER CARD IF
- SHEET19 - AIC33

- SHEET20 - DM9000A ENET CONTROLLER
- SHEET21 - ETHERNET CONNECTOR
- SHEET22 - MSP430
- SHEET23 - LEDS/SWITCHED ETC
- SHEET24 - I/O DAUGHTER CARD IF
- SHEET26 - CORE PWR SUPPLY,MSP430 PWR SUPPLY
- SHEET27 - 3V3 AND 1V8 POWER SUPPLY

REVISION STATUS OF SHEETS

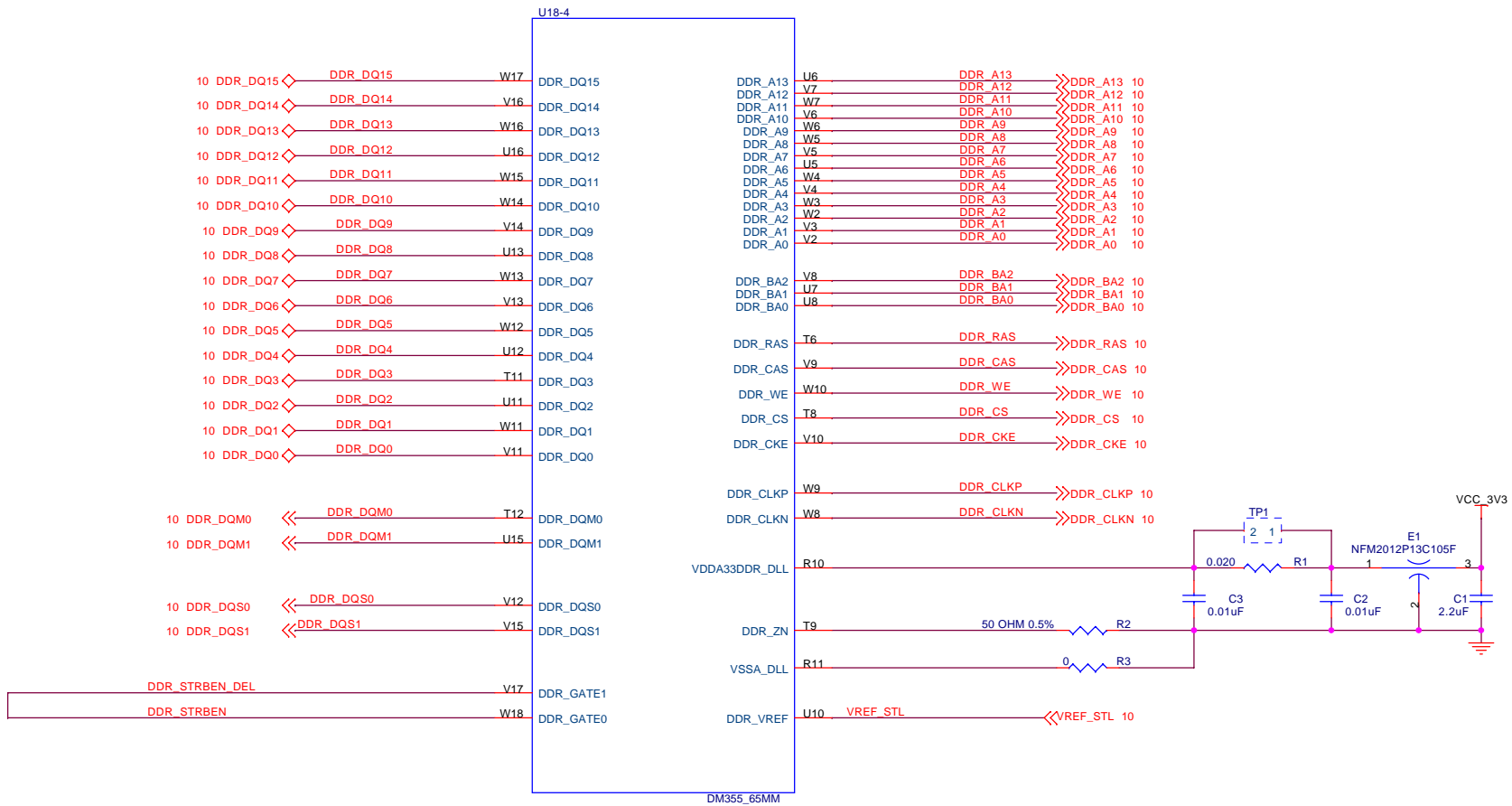
REV	DATE	DESCRIPTION	BY	CHK	DATE	DESCRIPTION	BY	CHK	DATE	DESCRIPTION	BY	CHK	DATE
A	04/01/2007	Initial schematic ready for layout - Alpha Release	DWN	RRP	04/01/2007	Pre-production release - Beta Release	CHK	T.W.K.	04/01/2007	Production release for 0.50 mm	ENGR	RRP	04/01/2007
B	07/01/07	Pre-production release - Beta Release	ENGR-MGR	RRP	04/01/2007	Pre-production release for 0.65 mm	ENGR	C.M.D.	04/01/2007	Production release for 0.50 mm	MFG	RRP	04/01/2007
C	09/01/07	Production release for 0.50 mm	RLSE	RRP	04/01/2007	Pre-production release for 0.65 mm	RLSE	RRP	04/01/2007	Production release for 0.50 mm	RLSE	RRP	04/01/2007

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Title: DM355 Evaluation Module			
Page Contents: TITLE SHEET			
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DM355_65MM

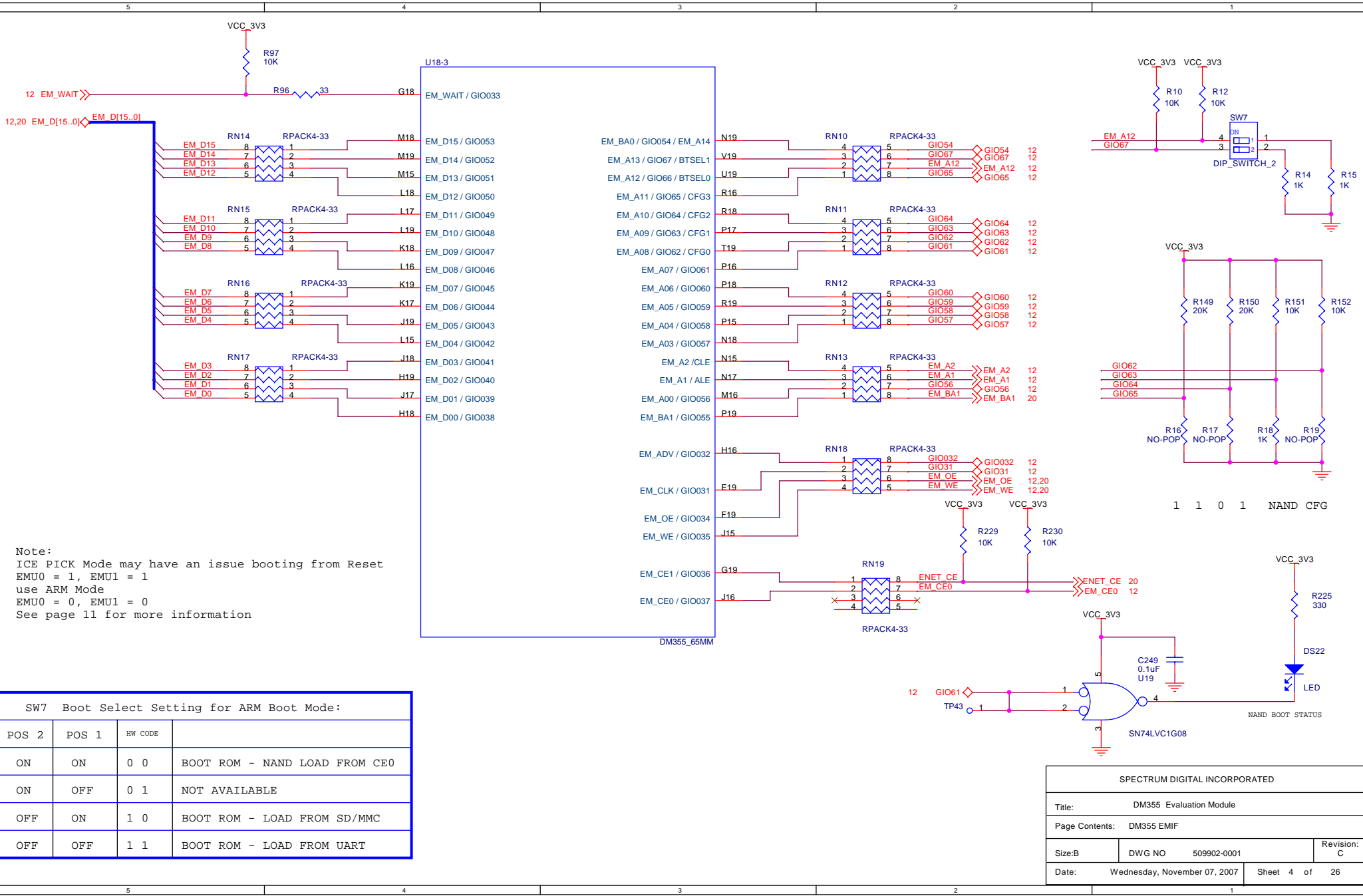
SPECTRUM DIGITAL INCORPORATED			
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Page Contents: DM355 SERIAL I/O			
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Trace to DDR memory
for delay compensation

This net is equal to the DDR_CLKP (or DDR_CLKN)
plus
the length of DDR_DQXX Average Trace length

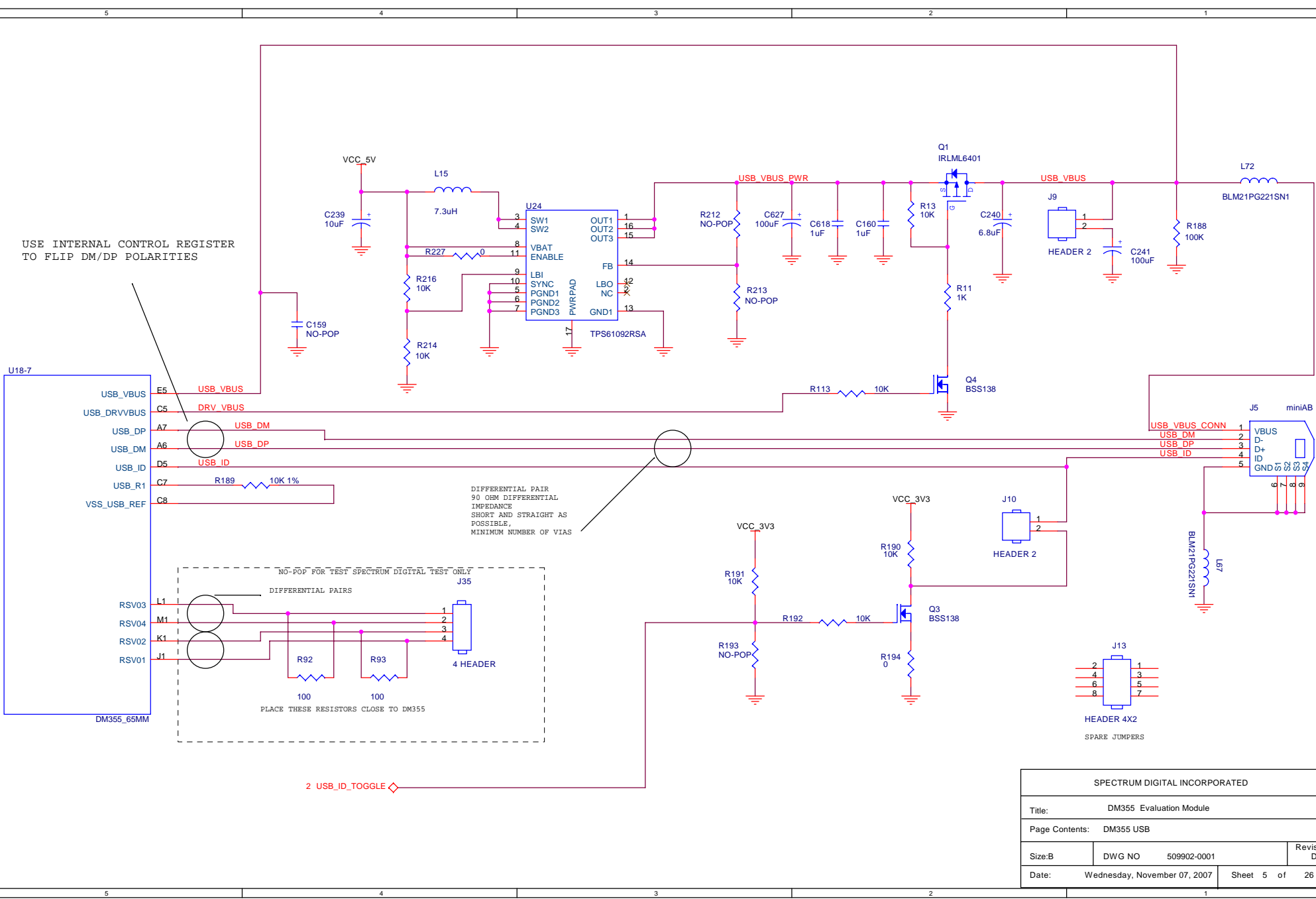
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Title: DM355 Evaluation Module			
Page Contents: DM355 DDR INTERFACE			
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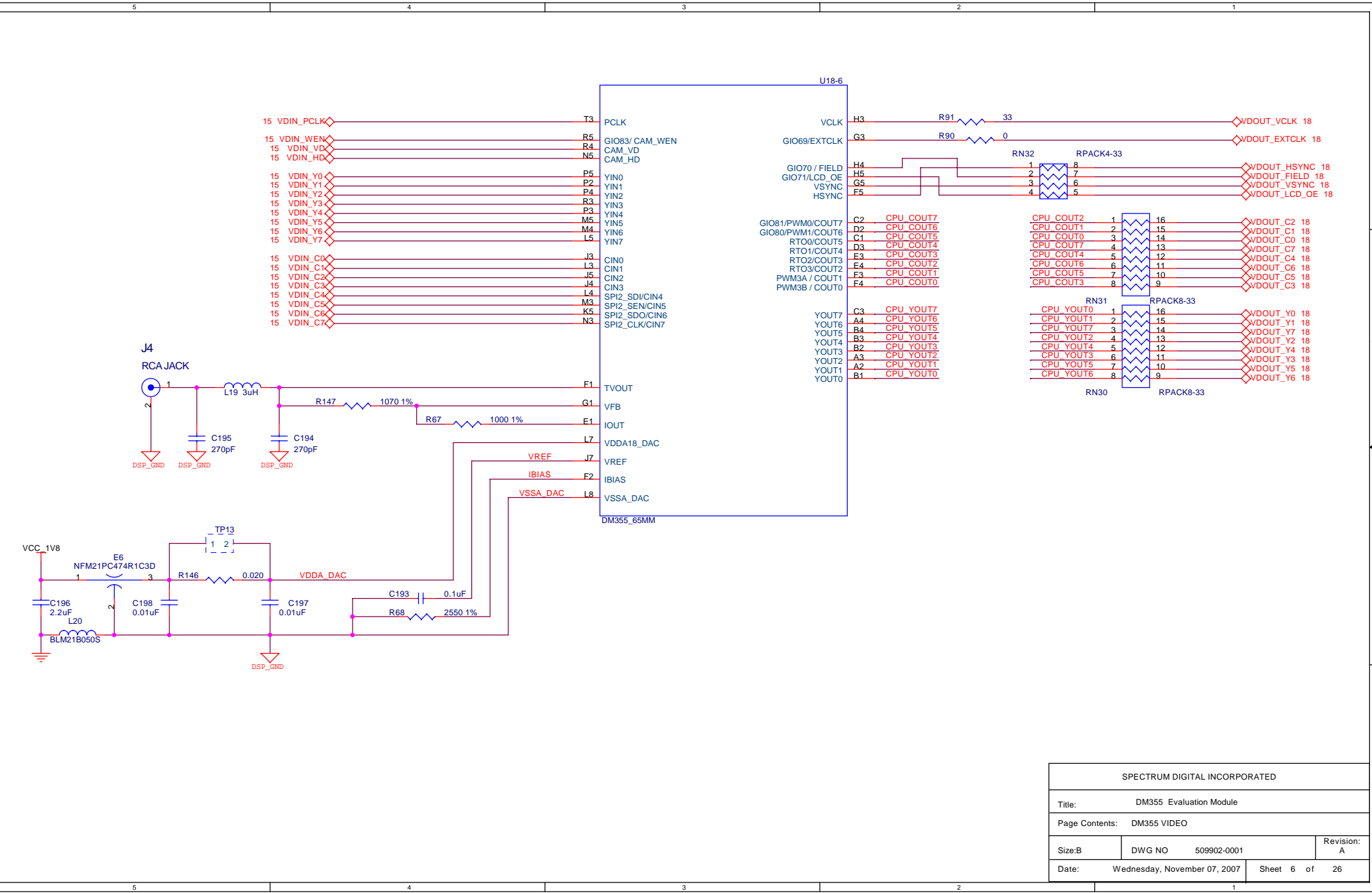
Note:
 ICE PICK Mode may have an issue booting from Reset
 EMU0 = 1, EMU1 = 1
 use ARM Mode
 EMU0 = 0, EMU1 = 0
 See page 11 for more information

SW7 Boot Select Setting for ARM Boot Mode:			
POS 2	POS 1	HW CODE	
ON	ON	0 0	BOOT ROM - NAND LOAD FROM CE0
ON	OFF	0 1	NOT AVAILABLE
OFF	ON	1 0	BOOT ROM - LOAD FROM SD/MMC
OFF	OFF	1 1	BOOT ROM - LOAD FROM UART

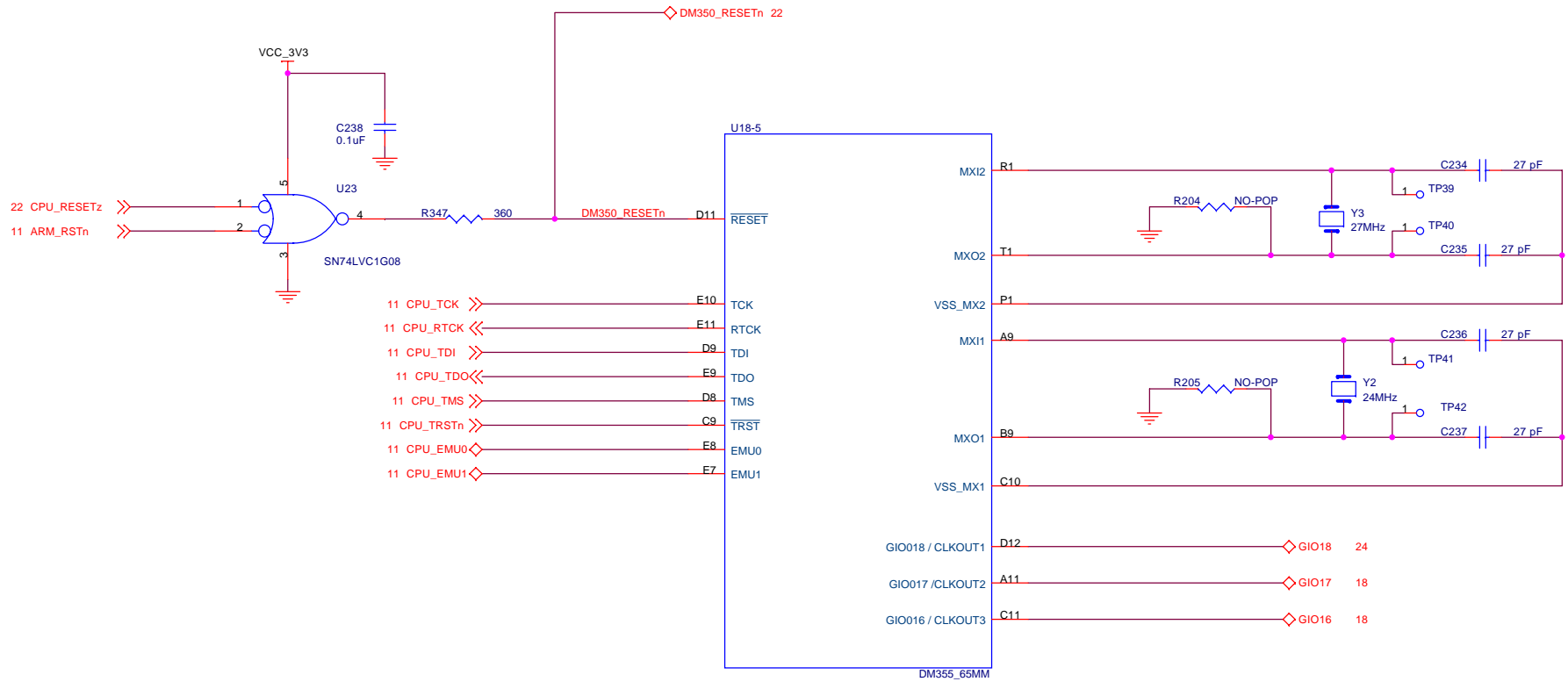
SPECTRUM DIGITAL INCORPORATED			
Title: DM355 Evaluation Module			
Page Contents: DM355 EMIF			
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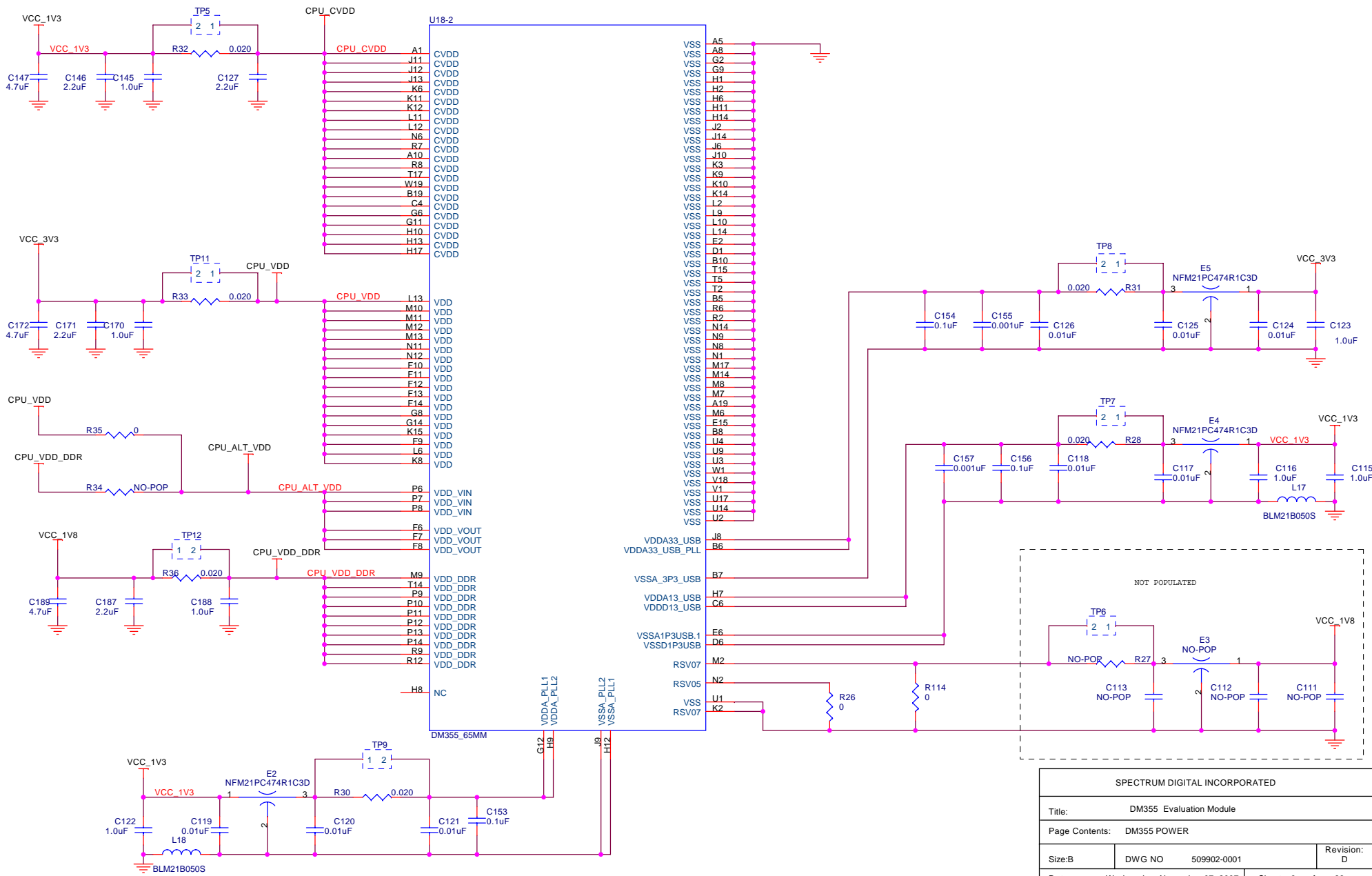
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Title: DM355 Evaluation Module			
Page Contents: DM355 USB			
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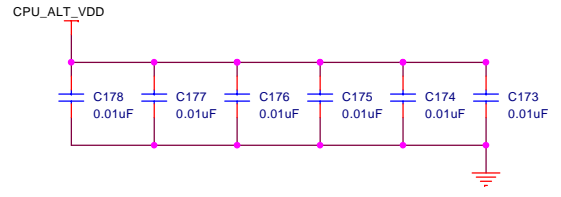
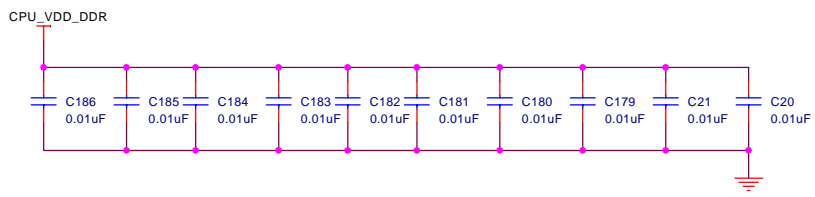
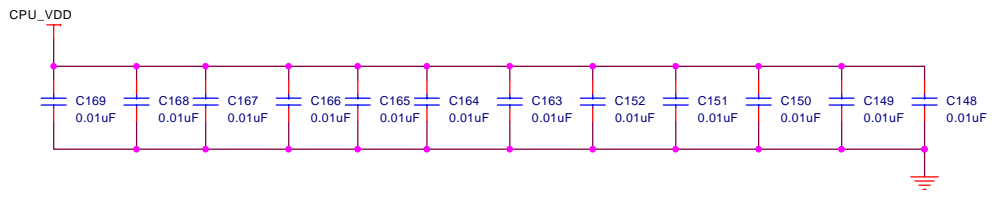
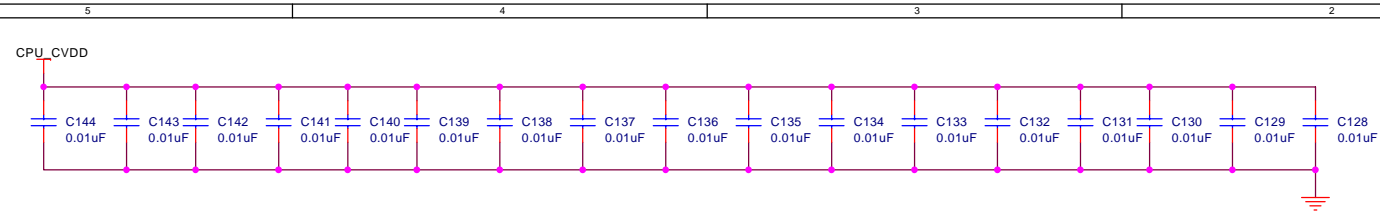
SPECTRUM DIGITAL INCORPORATED			
Title: DM355 Evaluation Module			
Page Contents: DM355 VIDEO			
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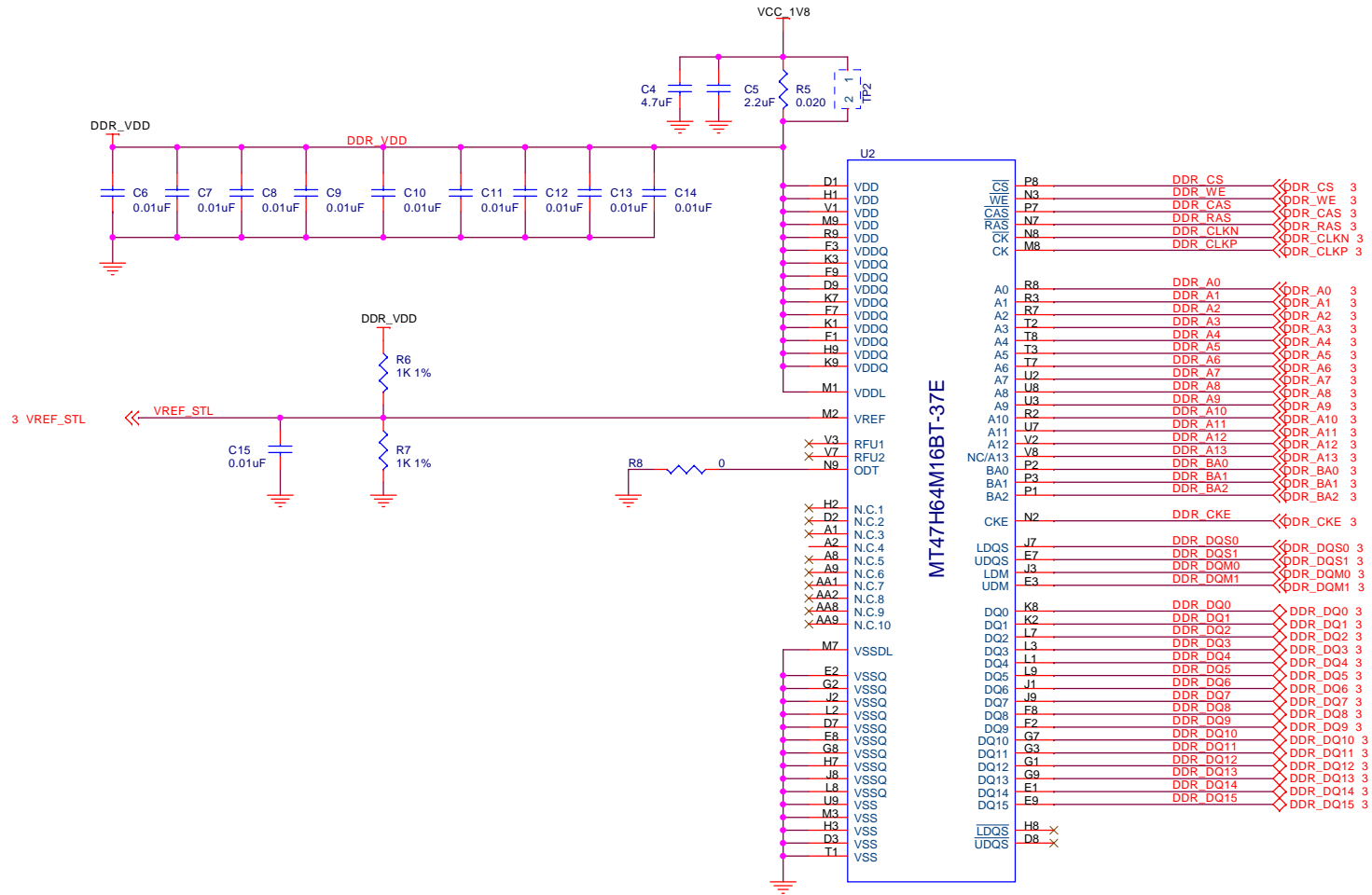
SPECTRUM DIGITAL INCORPORATED			
Title: DM355 Evaluation Module			
Page Contents: DM355 JTAG,RESET,CLOCKS			
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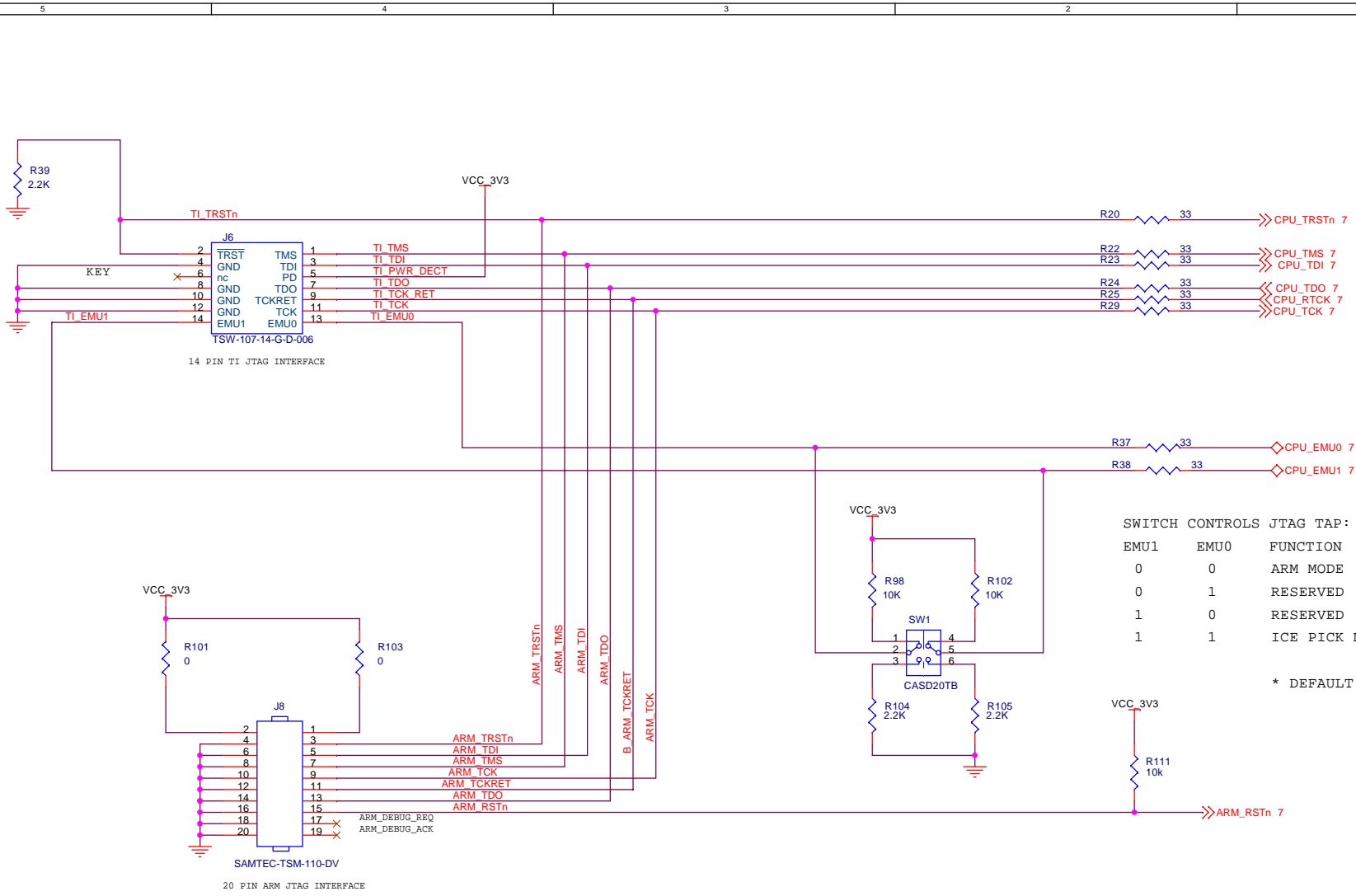
SPECTRUM DIGITAL INCORPORATED			
Title: DM355 Evaluation Module			
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Page Contents: DDR2 MEMORY			
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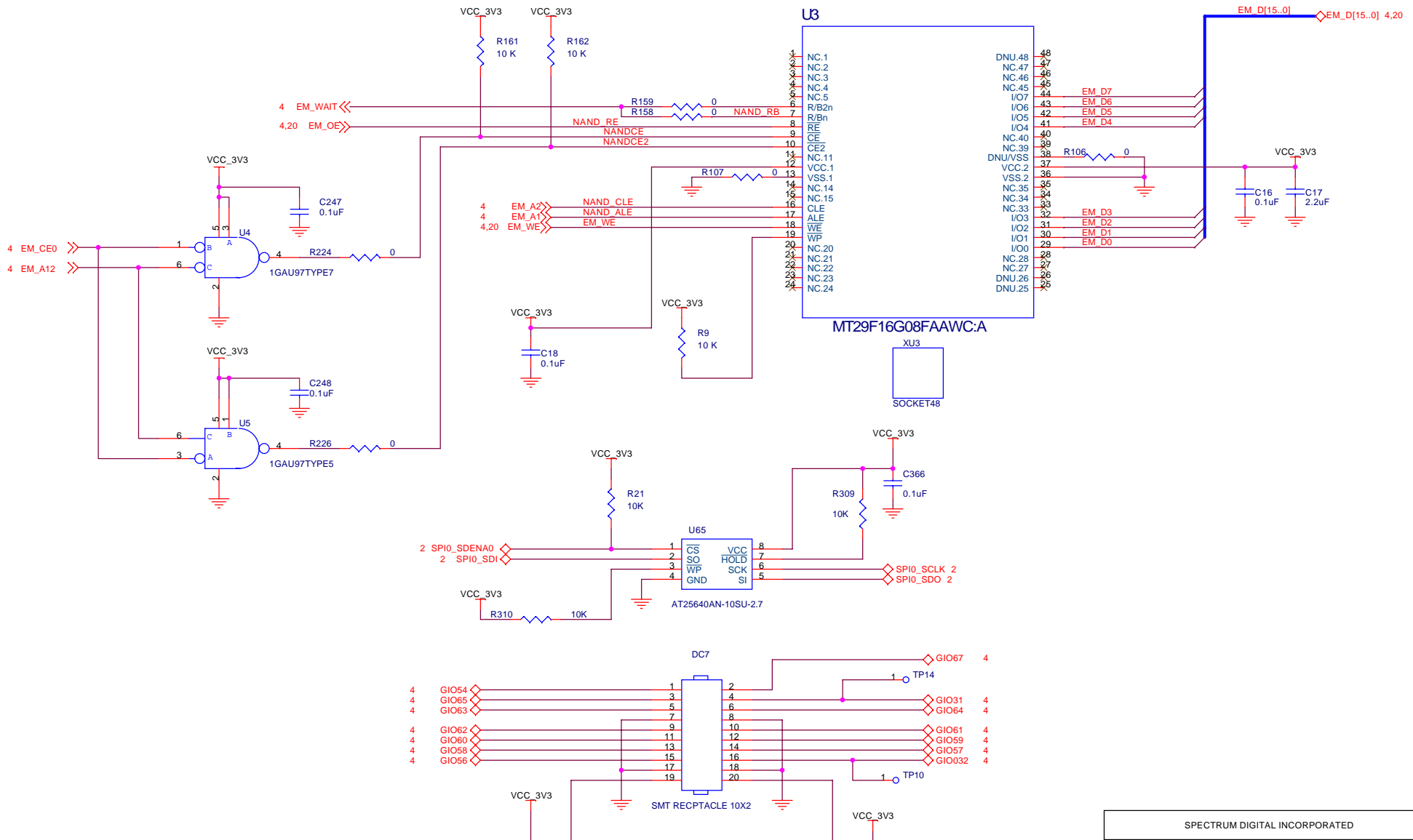


SWITCH CONTROLS JTAG TAP:

EMU1	EMU0	FUNCTION
0	0	ARM MODE
0	1	RESERVED
1	0	RESERVED
1	1	ICE PICK MODE *

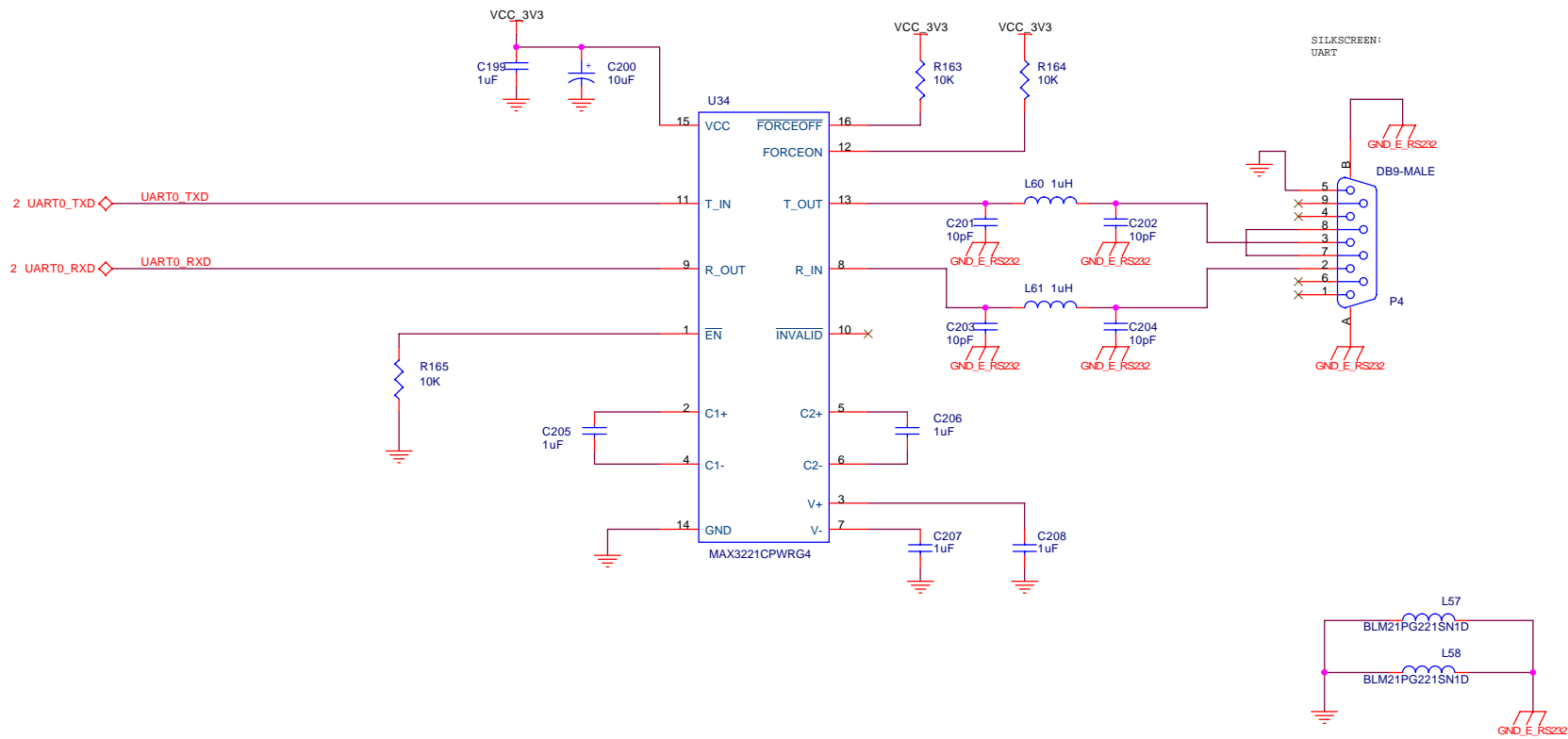
* DEFAULT

SPECTRUM DIGITAL INCORPORATED			
Title: DM355 Evaluation Module			
Page Contents: JTAG INTERFACE			
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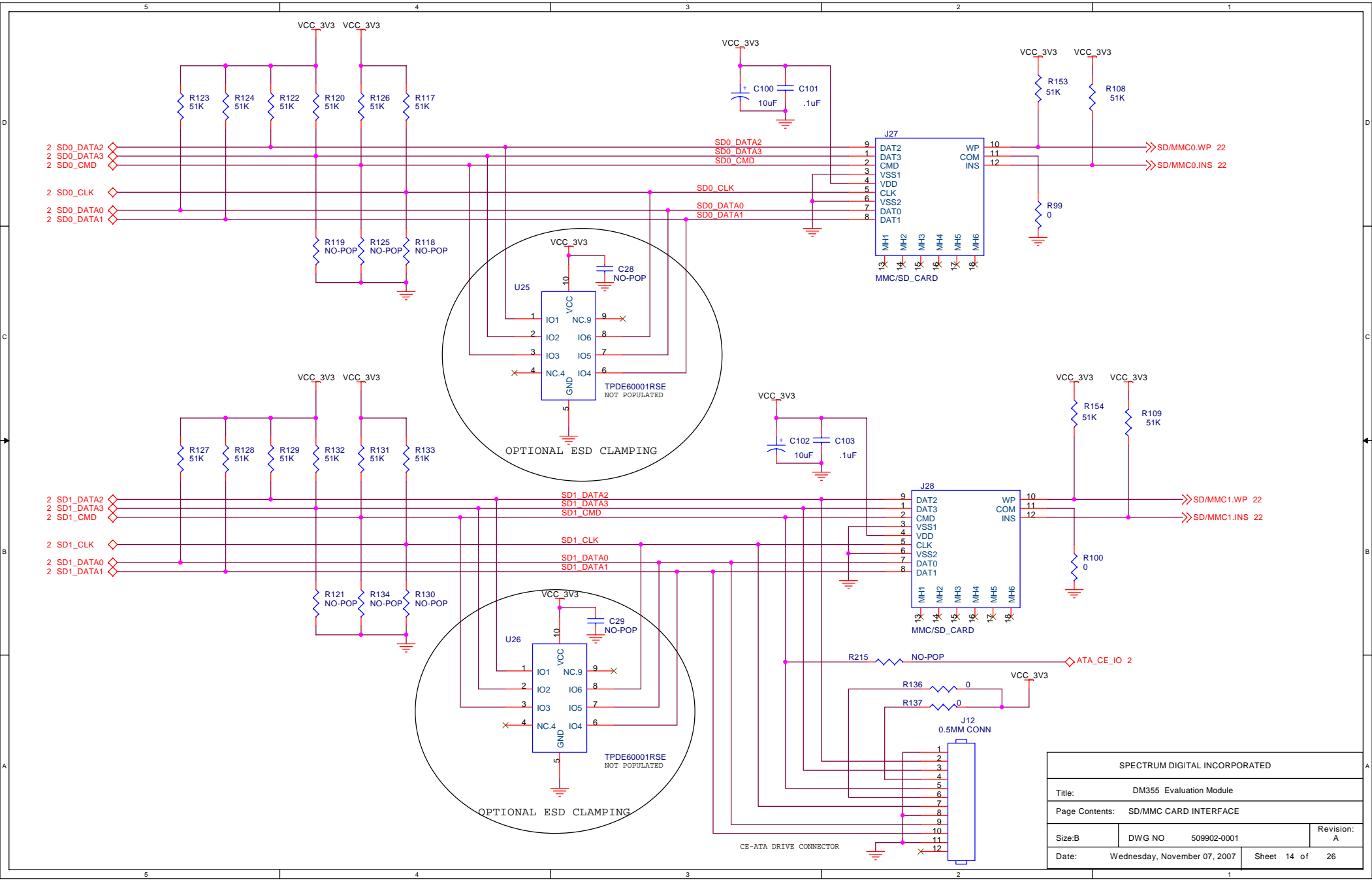
SPECTRUM DIGITAL INCORPORATED			
Title: DM355 Evaluation Module			
Page Contents: NAND FLASH, SPI EEPROM, EMIF I/O DC			
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5 4 3 2 1

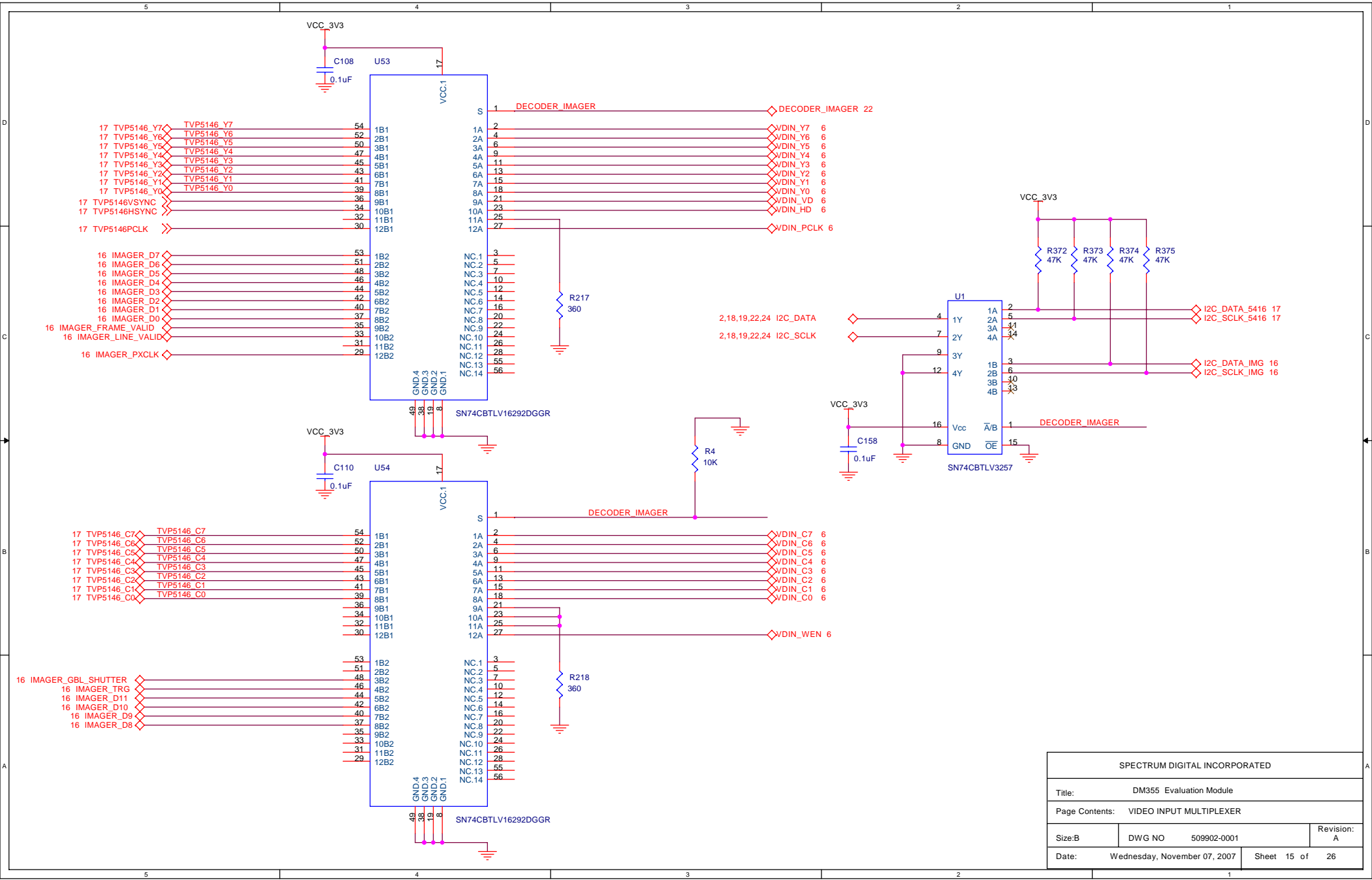


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Title: DM355 Evaluation Module			
Page Contents: RS232			
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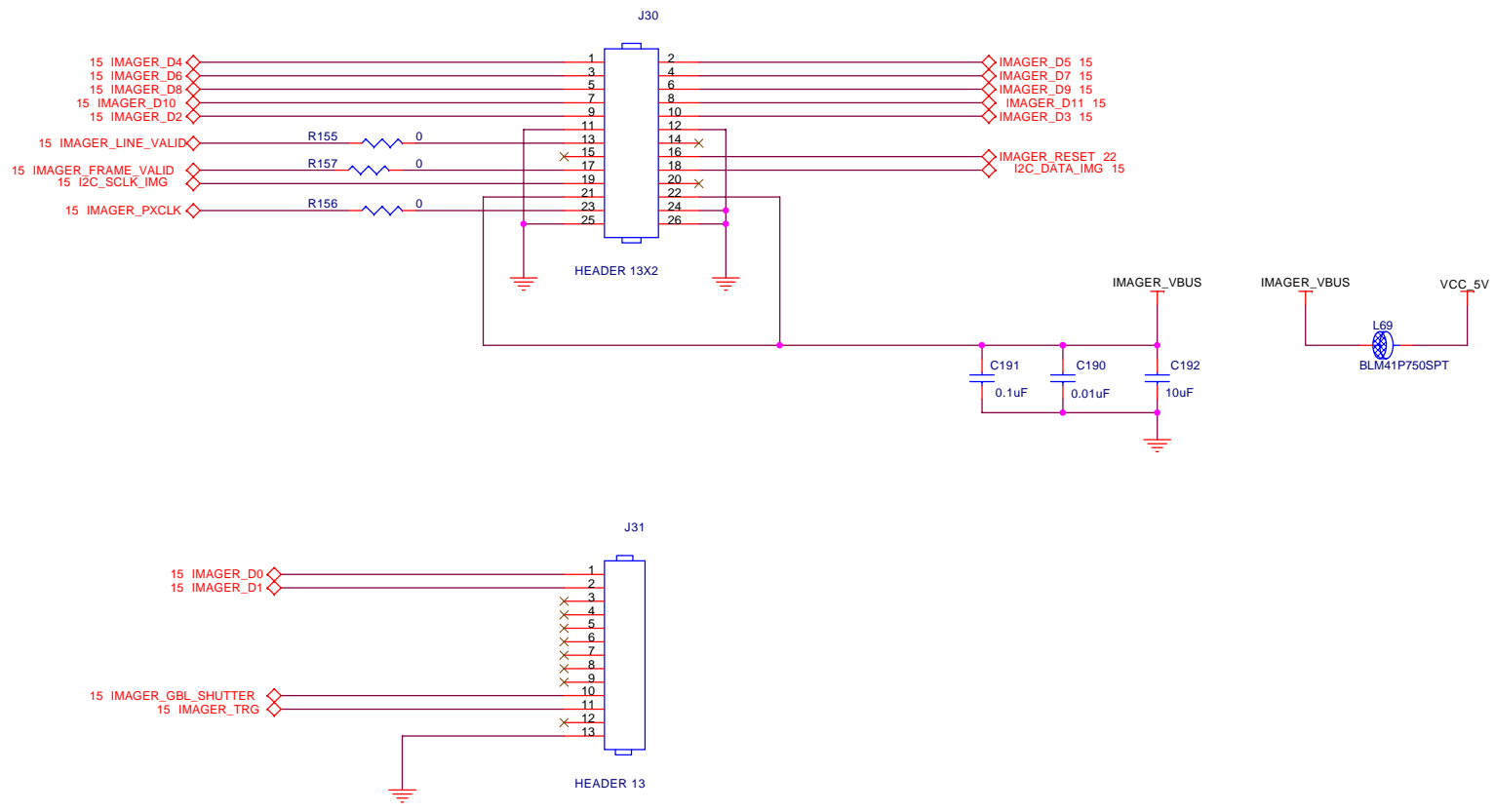
5 4 3 2 1



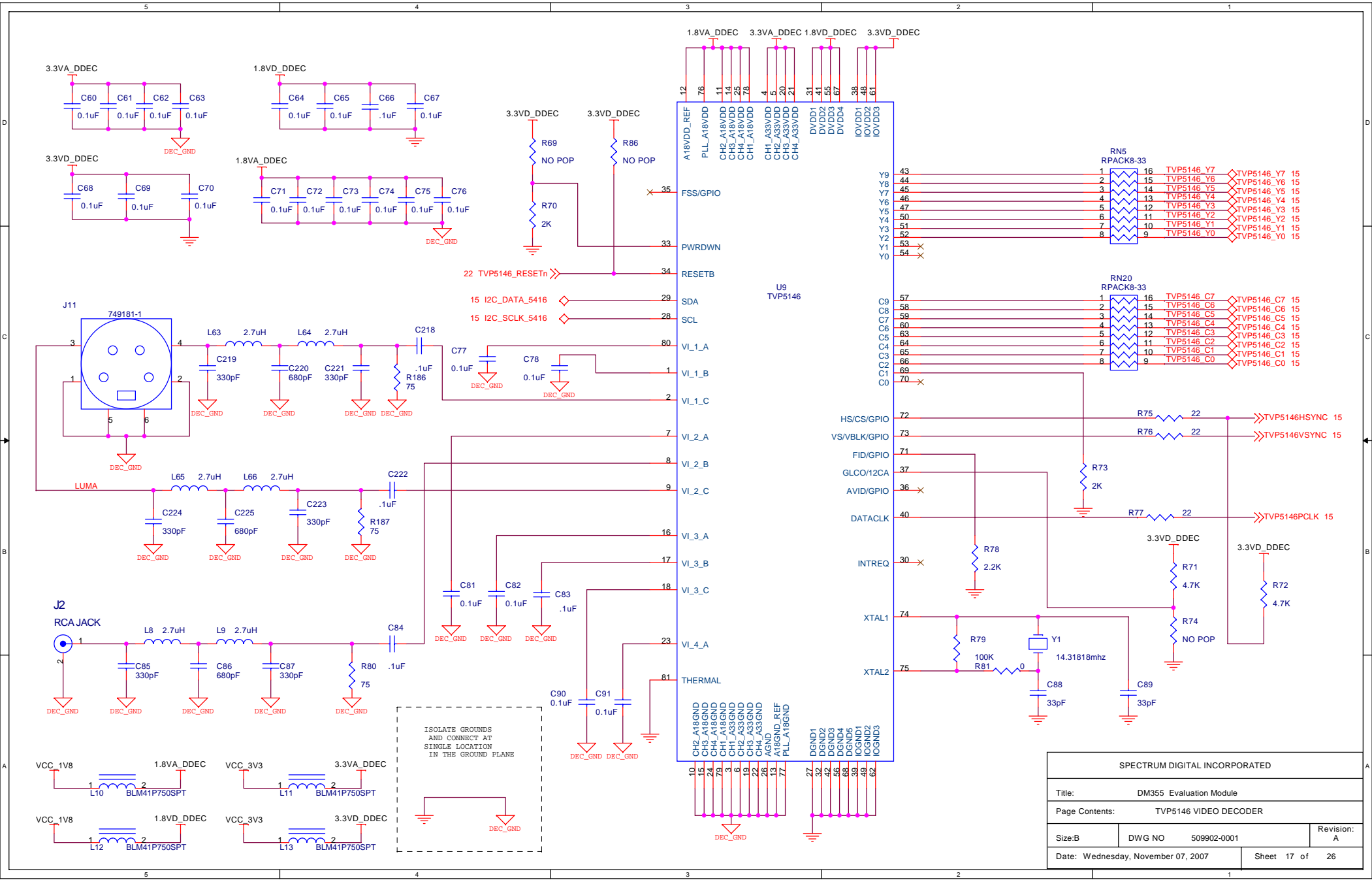
SPECTRUM DIGITAL INCORPORATED			
Title: DM355 Evaluation Module			
Page Contents: SD/MMC CARD INTERFACE			
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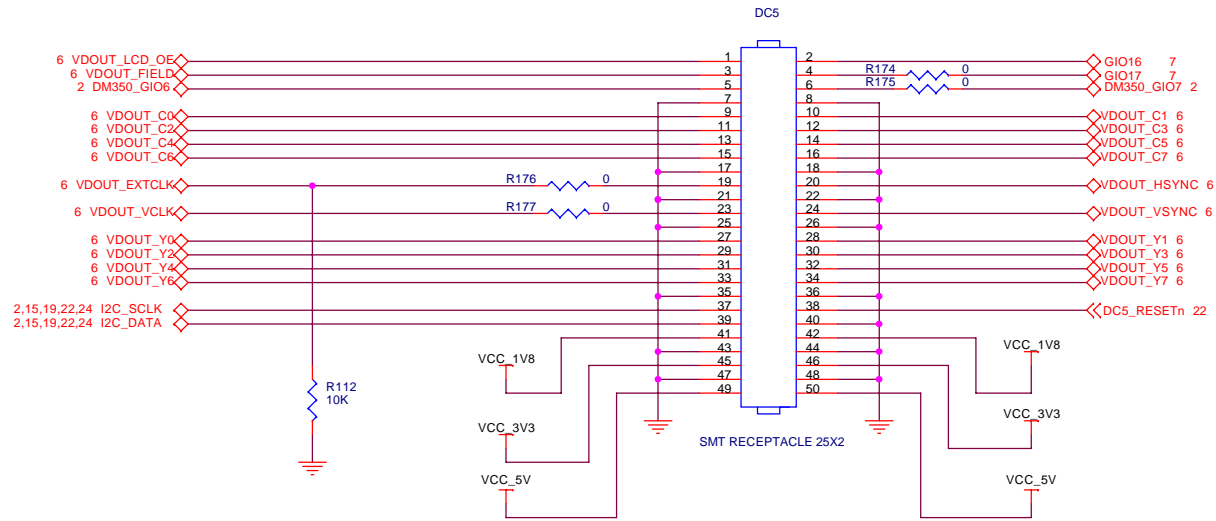
SPECTRUM DIGITAL INCORPORATED			
Title:		DM355 Evaluation Module	
Page Contents: VIDEO INPUT MULTIPLEXER			
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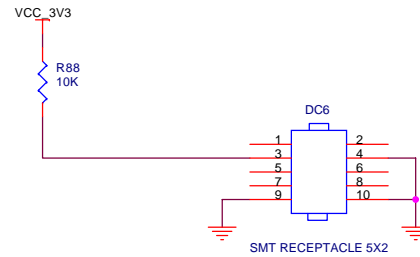
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Title: DM355 Evaluation Module			
Page Contents: IMAGER INTERFACE			
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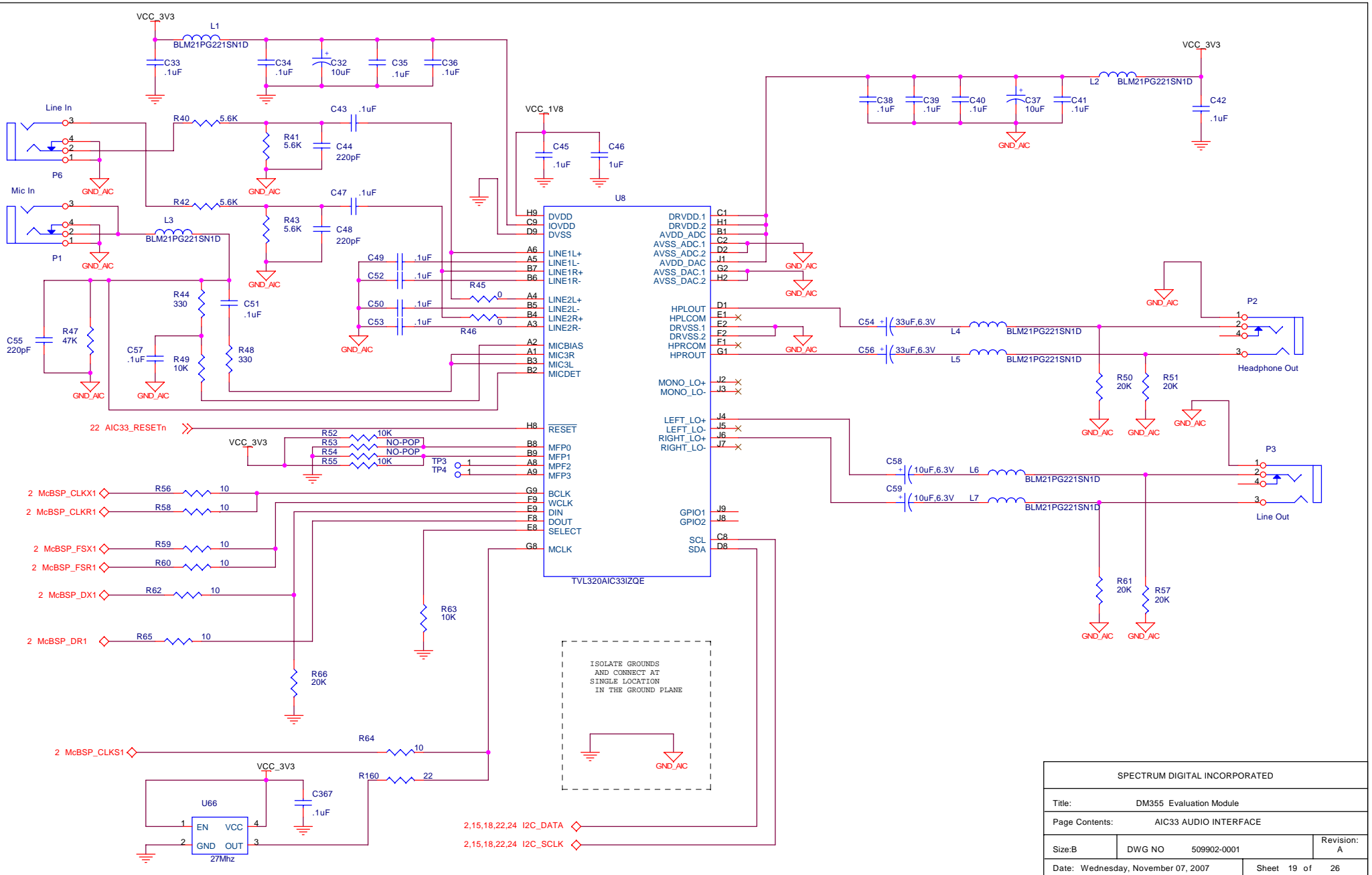
SPECTRUM DIGITAL INCORPORATED			
Title: DM355 Evaluation Module			
Page Contents: TVP5146 VIDEO DECODER			
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VIDEO OUTPUT CONNECTOR

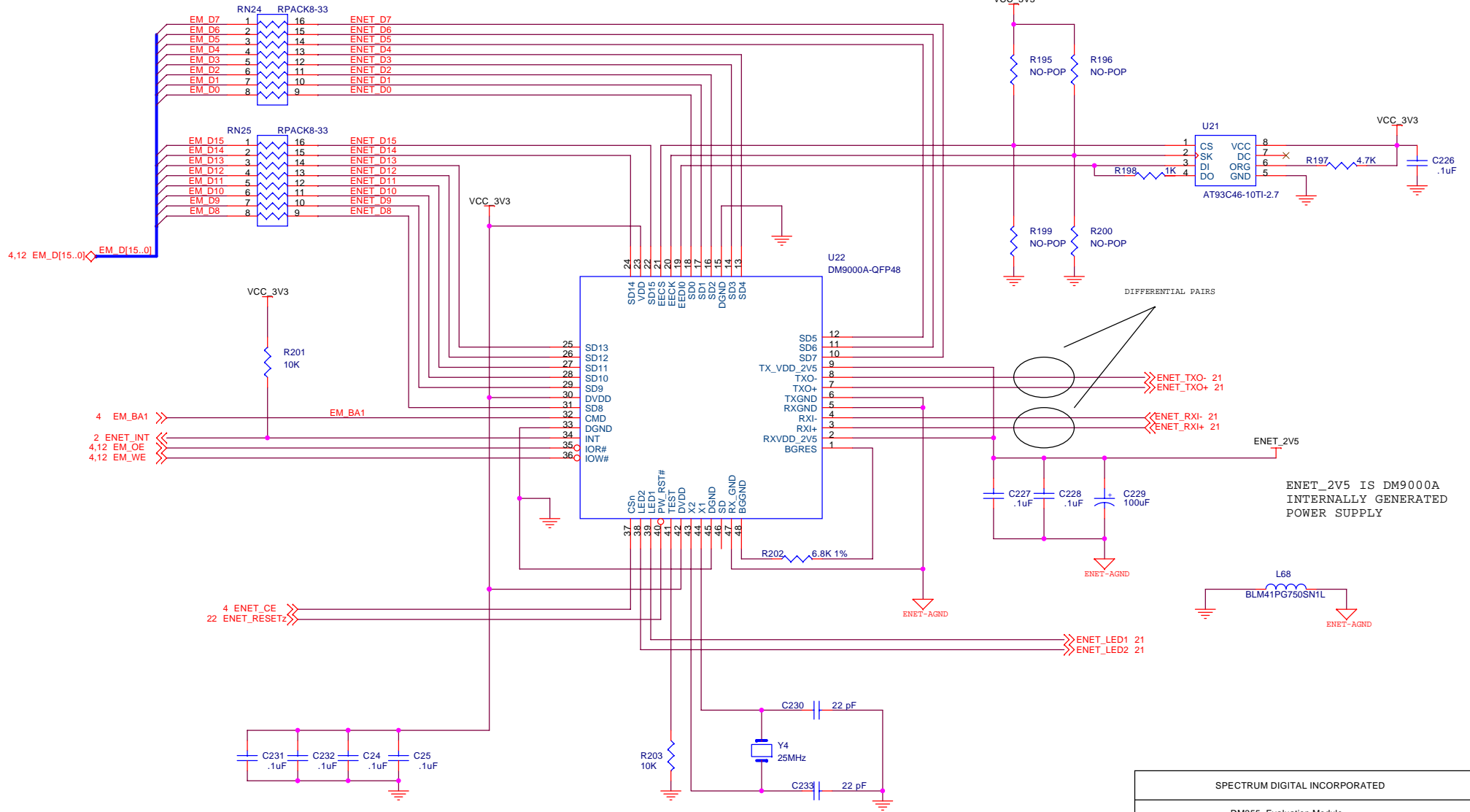


SPECTRUM DIGITAL INCORPORATED			
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Page Contents: THS8200 DAUGHTER CARD INTERFACE			
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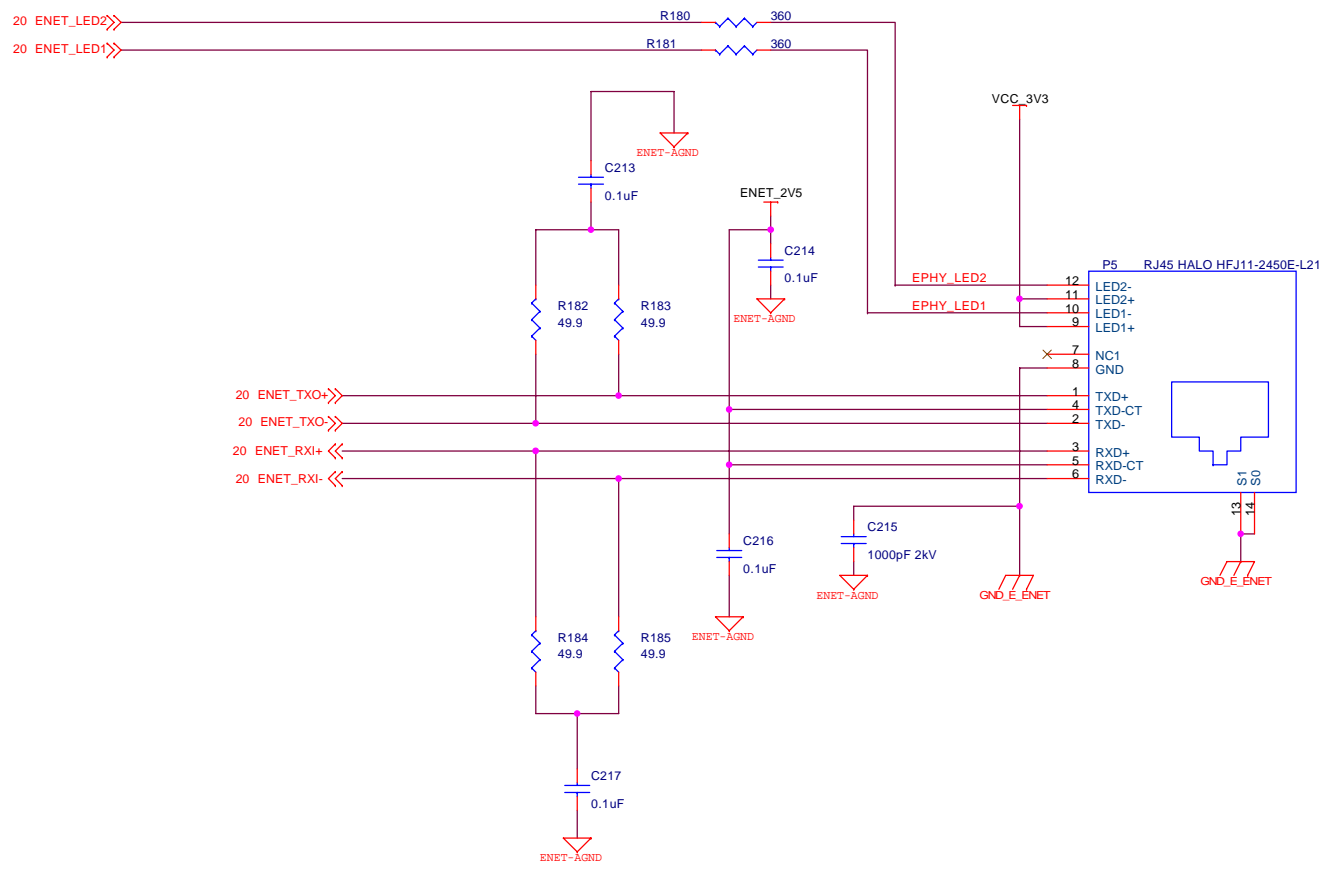


ISOLATE GROUNDS AND CONNECT AT SINGLE LOCATION IN THE GROUND PLANE

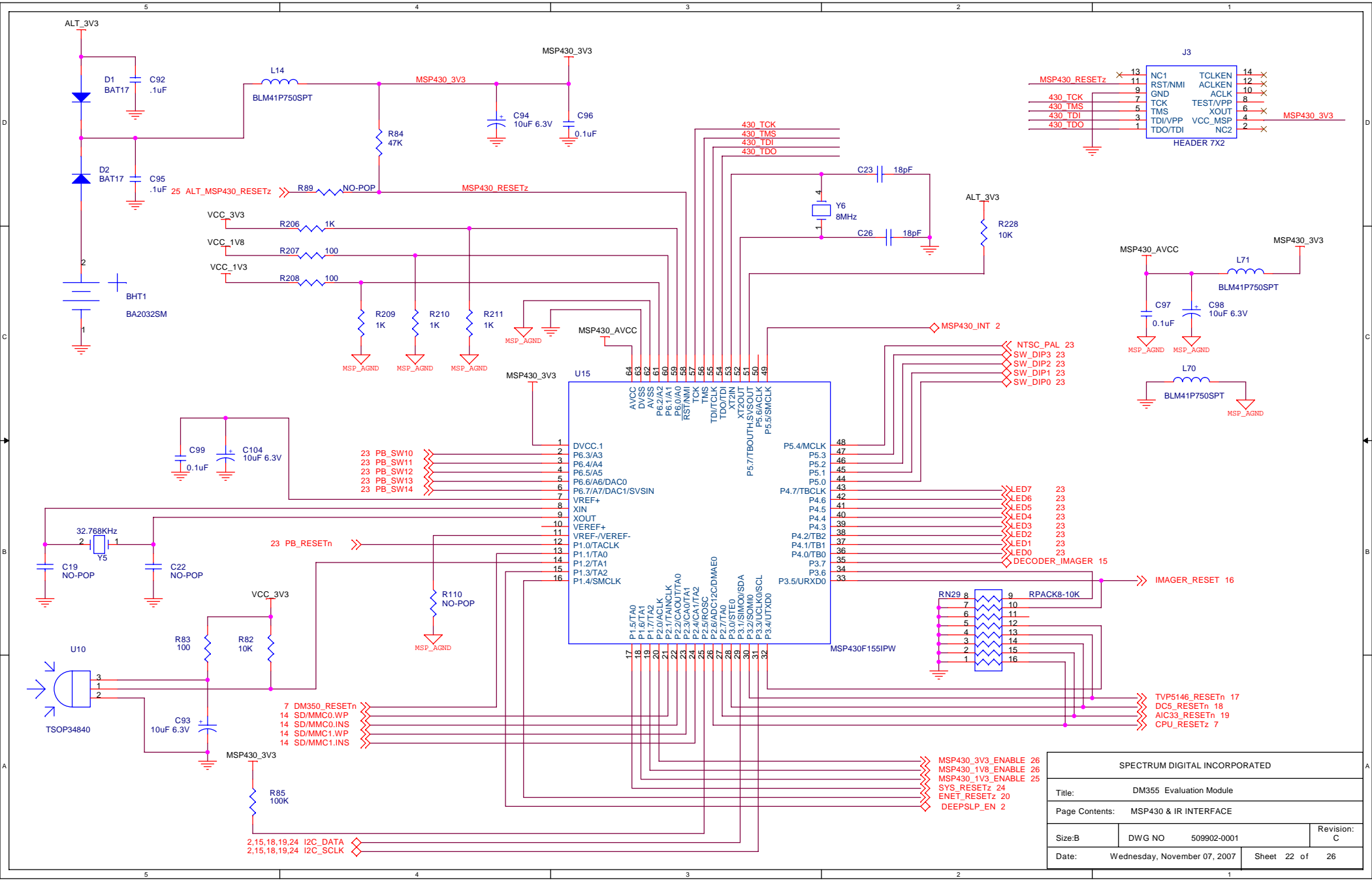
SPECTRUM DIGITAL INCORPORATED			
Title:		DM355 Evaluation Module	
Page Contents:		AIC33 AUDIO INTERFACE	
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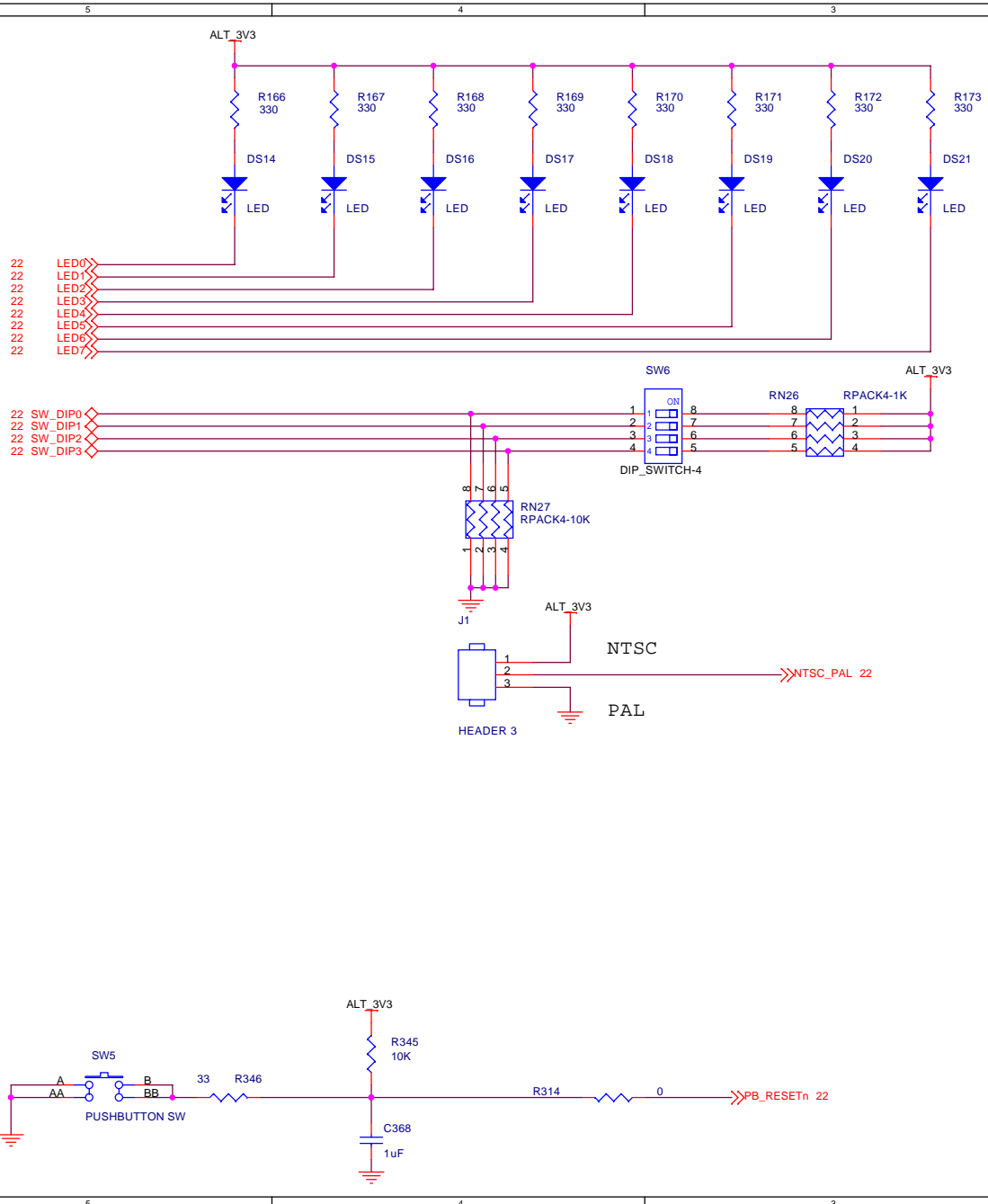
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Title: DM355 Evaluation Module			
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Title: DM355 Evaluation Module			
Page Contents: ETHERNET OUTPUT			
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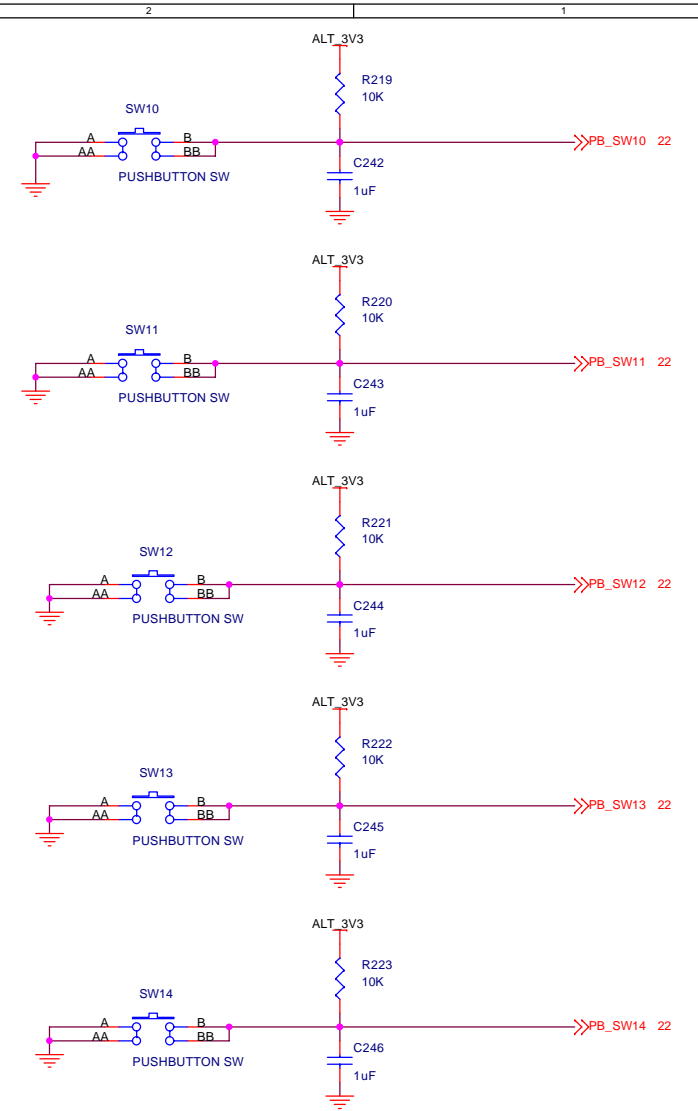


SPECTRUM DIGITAL INCORPORATED			
Title: DM355 Evaluation Module			
Page Contents: MSP430 & IR INTERFACE			
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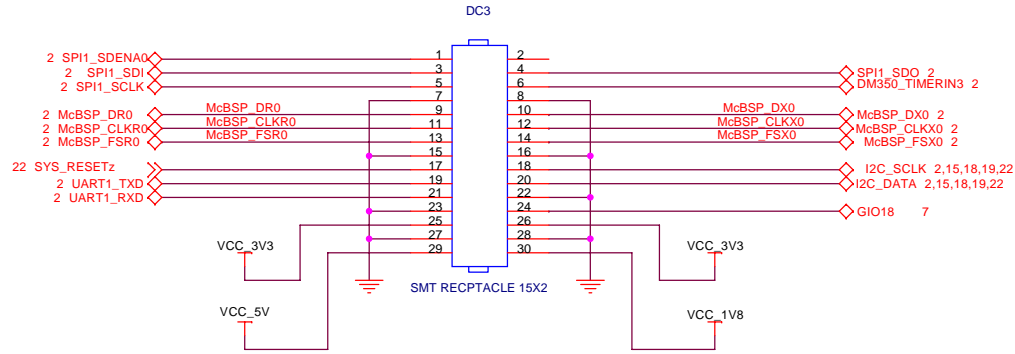


- 22 LED0
- 22 LED1
- 22 LED2
- 22 LED3
- 22 LED4
- 22 LED5
- 22 LED6
- 22 LED7

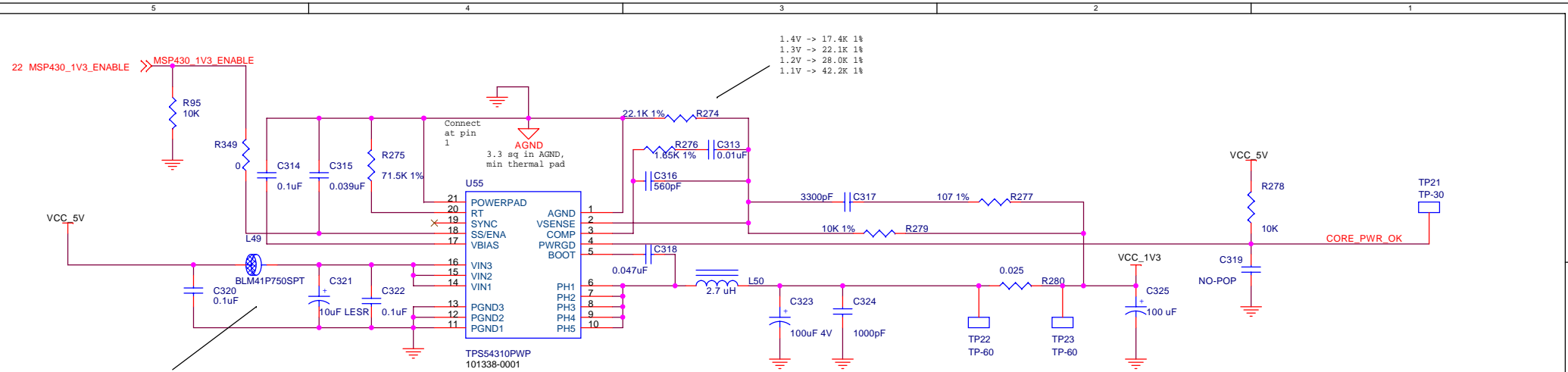
- 22 SW_DIP0
- 22 SW_DIP1
- 22 SW_DIP2
- 22 SW_DIP3



SPECTRUM DIGITAL INCORPORATED			
Title: DM355 Evaluation Module			
Page Contents: SWITCHES, LEDS ETC			
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1.4V -> 17.4K 1%
 1.3V -> 22.1K 1%
 1.2V -> 28.0K 1%
 1.1V -> 42.2K 1%

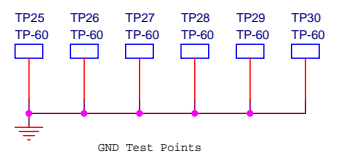
EMI SUPPRESSION. LOCATE NEAR EACH REGULATOR. 6 VIAS FROM PAD TO PLANE OR DIRECT TIE.

$$V_{out} = V_{ref} * (1 + R_{1503}/R_{1504})$$

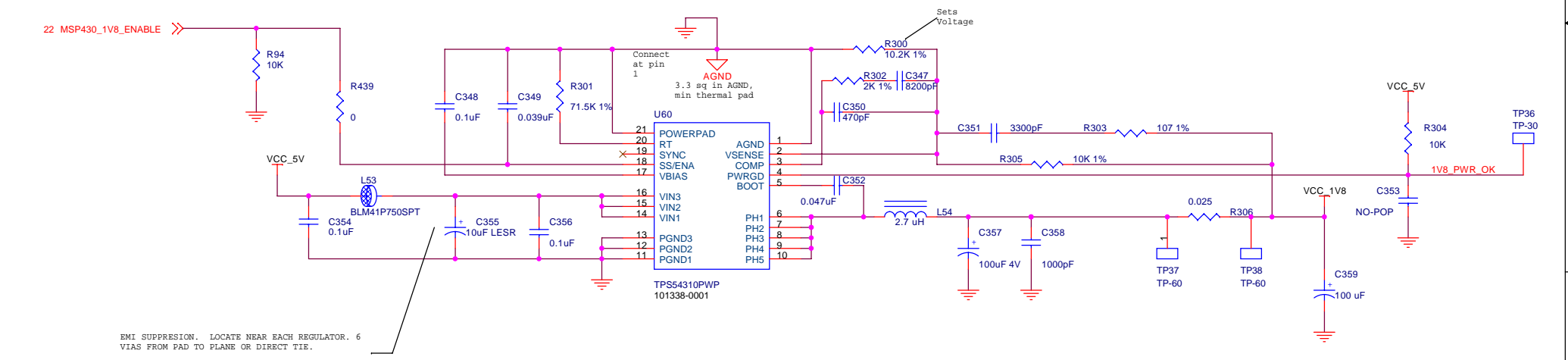
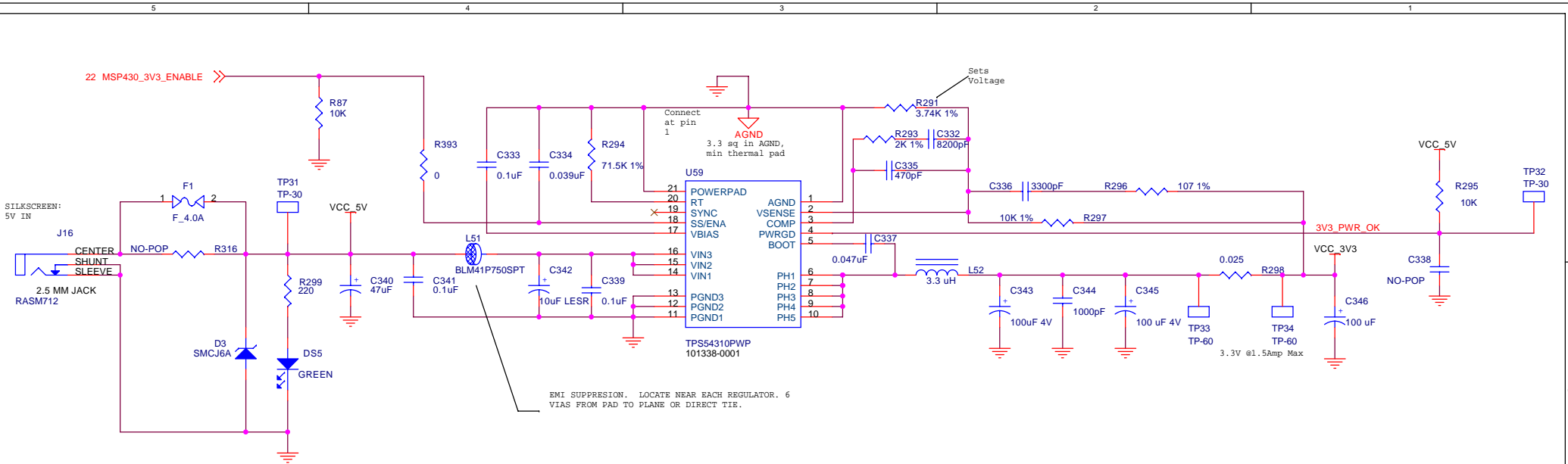
Vref = 1.182 Volts

Vout = 3.6 volts

R1503 = 346K



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Page Contents: POWER SUPPLY MSP430_3V3, DSP CORE(1V3)			
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